AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application.

24. (Currently Amended) A memory cell providing reading, writing, and storage of a data bit, said cell comprising:

a first transistor having a first source node, a first gate node, and a first drain node; and

a second transistor having a second drain node that is electrically connected to said first drain node, said second transistor having a second source node that is electrically floating, and a second gate node that is connected to a bias voltage level.

25. (Cancelled)

26. (Previously Presented) The cell of claim 24 wherein said first transistor is a field-effect-transistor (FET).

27. (Previously Presented) The cell of claim 24 wherein said second transistor is a FET.

28. (Previously Presented) The cell of claim 24 wherein said first drain node and said second drain node, connected together, constitute a storage node.

29. (Previously Presented) The cell of claim 24 further comprising a pulsed voltage driver connected to said second gate node.

30. (Previously Presented) The cell of claim 24 wherein said first gate node comprises a memory read/write-enable line.

31. (Previously Presented) The cell of claim 24 wherein said first source node comprises a memory bit line that is written to and read from.

32. (Previously Presented) The cell of claim 24 wherein said second transistor has a first storage capacitance associated with a junction of said second transistor and a second storage capacitance associated with an oxide layer of said second source node to store said data bit.

33. (Previously Presented) A method for reducing leakage current when storing a data bit in an embedded memory cell, said method comprising:

writing a data bit to a memory cell during a first time segment;

applying a transistor disabling reference ground potential to a first gate node of a first transistor of said memory cell during a second time segment;

applying a first reference voltage to a first source node of said first transistor during said second time segment; and

applying a second reference voltage to a second gate node of a second transistor during at least a portion of said second time segment.

34. (Previously Presented) The method of claim 33 wherein said second time segment is after said first time segment.

35. (Previously Presented) The method of claim 33 wherein said writing comprises:

applying a first voltage to said first source node of said first transistor during said first time segment;

applying a second voltage level, with respect to said reference ground potential, to said first gate node of said first transistor during said first time segment; and

applying said second voltage level to said second gate node of said second transistor during at least said first time segment.

36. (Previously Presented) The method of claim 35 wherein said first voltage is a data bit voltage.

37. (Currently Amended) The method of claim 35 wherein said second voltage level is a read/write enabling voltage.

38. (Previously Presented) The method of claim 35 wherein said second voltage level is equal to said first reference voltage.

39. (Previously Presented) The method of claim 35 wherein said second voltage level is more positive than said first reference voltage.

40. (Previously Presented) The method of claim 33 wherein said second reference voltage is more positive than said first reference voltage.

41. (Previously Presented) The method of claim 33 wherein a first drain node of said first transistor is electrically connected to a second drain node of said second transistor.

42. (Previously Presented) The method of claim 33 wherein a second source node of said second transistor is electrically floating.

43. (Previously Presented) The method of claim 33 wherein said first transistor is a FET.

44. (Previously Presented) The method of claim 33 wherein said second transistor is a FET.

45. (Previously Presented) The method of claim 33 wherein said second transistor has a first storage capacitance associated with a junction of said second transistor and a second storage capacitance associated with an oxide layer of a second source node of said second transistor to store said data bit.

46. (Previously Presented) The method of claim 33 wherein said data bit is represented by a voltage level corresponding to said reference ground potential.

47. (Previously Presented) The method of claim 33 wherein said data bit is represented by a voltage level that is more positive than said reference ground potential.